RUBEN REYES

Sunnyvale, California | Ruben.Reyes@AthenaCloudEngineers.com | (408) 857-4771

PRINCIPAL ASIC PHYSICAL DESIGN ENGINEER

EXECUTIVE PROFILE

Principal ASIC Physical Design Engineer with more than 30 years of semiconductor engineering experience and 19+ tape-outs, spanning IBM Research through advanced-node SoC implementation at leading technology companies. Hands-on technical leader with end-to-end expertise from synthesized RTL/netlist through foundry-ready GDSII, including floorplanning, placement, CTS, routing, STA, timing closure, ECO, power integrity, low-power implementation, physical verification and signoff.

Experienced in owning difficult physical-design problems at block and chip level, developing implementation and signoff methodology, debugging SDC/UPF and multi-corner timing issues, driving PPA convergence, and working across design, CAD, timing, power and verification teams. Advanced-node experience includes TSMC designs down to 4nm and extensive use of Synopsys and Cadence implementation/signoff platforms.

Brings a research and methodology background from IBM, Synopsys and Cadence together with decades of production tape-out experience. Uses Tcl, Python and shell automation to improve repeatability, debug efficiency and engineering productivity. Machine-learning and AI education complements the core physical-design background and supports development of AI-assisted EDA and engineering automation.

PRINCIPAL-LEVEL PHYSICAL DESIGN CAPABILITIES

- RTL / Netlist to GDSII Ownership: floorplanning, placement, CTS, routing, optimization, ECO, physical verification, signoff and tape-out.
- Timing Closure & STA: PrimeTime, Tempus, SDC, MMMC, setup/hold closure, clock-path analysis, WNS/TNS reduction, timing ECO and constraint development/debug.
- Advanced-Node Implementation: hands-on experience across multiple technology generations, including TSMC down to 4nm, with complex high-performance and low-power SoCs.
- Power & Power Integrity: PrimePower/PT-PX, Voltus, RedHawk, dynamic/leakage analysis, vector-based power, IR/EM analysis and power-grid implementation.
- Low-Power Design: UPF, multiple power domains, isolation, retention, level shifters and power-intent debugging.
- Physical Verification & Signoff: Calibre, IC Validator/VUE, DRC, LVS, ERC, DFM, antenna and tape-out readiness.
- Methodology & Automation: Tcl, Python, shell, Makefile, SED/AWK; design-flow automation, report analysis and implementation/signoff methodology.
- Technical Leadership: cross-functional problem solving, multi-team coordination, design reviews, methodology development, mentoring and execution under tape-out schedules.

EDA / TECHNOLOGY EXPERTISE

Synopsys: Fusion Compiler, ICC2, Design Compiler, PrimeTime, PrimeTime-SI, PrimePower/PT-PX, Formality, StarRC, IC Validator/VUE

Cadence: Innovus, Tempus, Genus, Voltus, Conformal, Xcelium, Verdi, Virtuoso, First Encounter, SKILL

Other: RedHawk, Calibre, FlowTracer, CVS, Perforce, ClearCase, Git, LSF

Designs: CPU/PowerPC, DDR PHY/DDR5, graphics, AI/ML compute, NOC, VP9/H.264, GDDR, PCIe/PCI-X, RFID, voice-recognition IP, mixed-signal and test chips

Process: TSMC down to 4nm; Intel, Samsung, GlobalFoundries, UMC, Chartered and IBM technologies

AI / ML: Python, NumPy, Pandas, Scikit-learn, Jupyter, Colab, Kaggle, Hugging Face, Ollama, ChatGPT, Gemini, Microsoft Copilot

PROFESSIONAL EXPERIENCE

ATHENA CLOUD ENGINEERS, LLC — Sunnyvale, CA

Principal ASIC Physical Design Engineer / Consultant | Apr 2019 – Present

Provide principal-level ASIC physical-design, STA, power, low-power and signoff engineering services. Lead and resolve complex implementation problems across advanced-node designs, with emphasis on timing convergence, SDC/MMMC, UPF, power analysis, IR/EM, physical verification and tape-out execution.

Selected Client Engagements

AMAZON

ASIC Physical Design Engineer — STA / SDC | May 2026 – Sep 2026

- Developed and verified static timing analysis (STA) and SDC constraints for advanced ASIC designs within a collaborative timing and physical-design environment.
- Performed PrimeTime timing analysis and debug, including setup/hold path analysis, constraint validation, clock-path behavior and timing-closure investigation.
- Supported physically aware ECO optimization and timing closure, analyzing residual setup and hold violations and coordinating fixes with implementation flows.
- Reviewed and validated SDC quality and timing intent to improve signoff correlation and reduce constraint-related timing issues.
- Applied Tcl-based analysis and automation to improve timing-debug efficiency, reporting and repeatability.

META

ASIC Physical Design Engineer / ASIC Power Engineer | Sep 2022 – Sep 2024

- Worked on TSMC 4nm physical-design and power flows using Cadence Innovus and Synopsys Fusion Compiler.
- Evaluated RTL and implementation tradeoffs for timing, power and area; debugged SDC, UPF, congestion and IR/EM issues.
- Developed Tcl/Python automation and authored internal physical-design and power methodology documentation.
- Coordinated technical work across multiple engineering teams to resolve implementation and signoff issues.

MAXENTRIC

ASIC Physical Design Engineer | Jan 2021 – Sep 2022

- Resolved late-stage physical-design and STA issues approaching tape-out in collaboration with the PD team.
- Developed solutions for SDC/clocking issues, created Structured Design Placement files and analyzed bottom-up constraints with Tempus and Genus.

GOOGLE

ASIC Physical Design / Power Engineer | Feb 2021 – Feb 2022

- Performed PrimePower analysis on TSMC 5nm designs and integrated Xtensa/Xcelium activity flows.
- Automated power-analysis workflows using Bash and FlowTracer.

SYNOPSYS

ASIC Physical Design Engineer | Feb 2021 – Jul 2021

- Led RTL-to-GDS implementation and tape-out activities for 5nm DDR5 designs.
- Performed timing/constraint analysis, EM/IR verification and DRC/LVS debugging using Synopsys implementation and signoff tools.

MICROSOFT

ASIC Physical Design Engineer | Jan 2021 – Jun 2021

- Led timing-constraint fixes and STA analysis on TSMC 5nm blocks using Innovus and PrimeTime.
- Performed power and rail analysis with PT-PX and Voltus, DRC/LVS with Calibre, and Tcl-based flow automation.

BROADCOM

ASIC Power Engineer | Dec 2019 – Jun 2021

- Developed UPF power intent and automated power-analysis workflows using Tcl and SQLite.
- Performed PrimeTime-PX and RedHawk power analysis.

EARLIER ASIC PHYSICAL DESIGN & LEADERSHIP EXPERIENCE

ESPERANTO TECHNOLOGIES — Sunnyvale, CA

ASIC Physical Design Engineer | Jan 2019 – Dec 2019

- Implemented and optimized a 26M-gate, ~1GHz TSMC 7nm NOC block, including floorplanning, timing and UPF.

ASTERA LABS — Sunnyvale, CA

ASIC Physical Design Verification Engineer | Jan 2019 – Mar 2019

- Performed full-chip DRC/LVS/antenna/DFM analysis and repair for tape-out.

INTEL — Sunnyvale, CA

ASIC Physical Design Engineer | Aug 2016 – Dec 2018

- Led advanced-node DRC/LVS debugging with IC Validator, developed Makefile automation, designed power/ground grids and supported floorplanning and timing convergence.

QUALCOMM — Sunnyvale, CA

ASIC Physical Design Engineer | Jun 2016 – Aug 2016

- Delivered netlist-to-GDSII implementation for mixed-signal designs and performed PrimeTime timing convergence/constraint optimization.

GOOGLE — Sunnyvale, CA

ASIC Physical Design Engineer | Mar 2015 – Jun 2016

- Led floorplanning and timing closure for VP9 encoder/decoder blocks; optimized six ~7M-gate blocks and reduced negative slack below approximately 100ps.

BROADCOM — Sunnyvale, CA

ASIC Physical Design Engineer | Nov 2015 – Jan 2016

- Performed full-chip STA under aggressive tape-out schedules and developed Tcl timing-report automation.

PNY TECHNOLOGIES — San Jose, CA

ASIC Physical Design Engineer | Jan 2015 – Nov 2015

- Evaluated Cadence and Synopsys implementation tool suites for SSD-controller design flows.

AMD — Sunnyvale, CA

Member of Technical Staff | Jul 2012 – Dec 2014

- Led timing closure, power integrity and RedHawk analysis across TSMC 32/28nm and GlobalFoundries 28/20nm; developed methodology and automation.

AMD — Sunnyvale, CA
ASIC Physical Design Engineer — Contract | Sep 2011 – Jul 2012
- Led PCIe implementation in a GDDR-based SoC; developed UPF low-power methodology and supported DFT scan-chain implementation.

SYNAPSE, INC. — Sunnyvale, CA
ASIC Physical Design Engineer | 2010
- Executed place-and-route, multi-corner timing/power optimization and tape-out support using Cadence/Synopsys flows.

CHIPSTART, LLC — Palo Alto, CA
Design Business Manager | Jun 2009 – Dec 2009
- Served as technical liaison across customers, sales, marketing and engineering for ASIC/IP delivery.

TRIVIUM TECH FORCE CORP. / GLOBAL TRIVIUM CORP. — Sunnyvale, CA
ASIC Design Manager | Jun 2008 – Jun 2009
- Led cross-functional ASIC teams, multi-site schedules, resource allocation, design reviews and project risk management.

QTHINK, INC. — San Jose, CA
ASIC Physical Design Engineer | 2004 – Jan 2008
Initially assigned to Arrow Electronics as a consultant and subsequently hired directly by QThink based on performance.
- Executed netlist-to-GDS physical design for consumer SoCs, including floorplanning, P&R, timing closure and DRC/LVS signoff.
- Used Cadence implementation tools for physical-design optimization and tape-out execution.

SYNOPSYS, INC. — Mountain View, CA
ASIC Physical Design Engineer | Aug 1998 – Sep 2003
- Supported customer ASIC engagements using Design Compiler, PrimeTime and Synopsys implementation technologies; developed/refined reference methodologies and guided RTL-to-GDS/timing-closure work.

CADENCE DESIGN SYSTEMS, INC. — San Jose, CA
ASIC Physical Design Engineer | Sep 1996 – Aug 1998
- Developed high-speed/low-power place-and-route solutions and SKILL automation to improve physical-design productivity.

IBM — Yorktown Heights, NY
Engineer — Research & Development | Dec 1982 – Jan 1996
- Conducted semiconductor and advanced CMOS R&D; contributed to microprocessor/ASIC design and methodology development; authored/co-authored patents and technical publications.

EDUCATION

Master of Science, Electrical Engineering — Polytechnic University, Brooklyn, New York, 1995

Bachelor of Science, Electrical Engineering, Honors — Pratt Institute, Brooklyn, New York, 1991

PROFESSIONAL EDUCATION & CERTIFICATIONS

- Cornell — Applied Machine Learning & Artificial Intelligence; Python Programming
- IBM Research — Advanced semiconductor, custom integrated-design and EDA training
- Synopsys — Project Management and advanced EDA tool training
- Cadence — Advanced EDA tool training
- De Anza College — Business Supervisory Management and Business Management
- Project Management Institute — Project Management Program
- Avanti — Advanced EDA tool training
- Cooper & Chyan Technology — IC Craftsman
- MAGMA — Advanced EDA tool training

PROFESSIONAL & TECHNICAL DISTINCTIONS

- IBM Research patents and publications
- Tau Beta Pi; IEEE; Eta Kappa Nu — President
- Pratt Institute Trustee & Chairman
- Authored technical papers
- Technical contributions to IBM products
- Semiconductor engineering, consulting and business leadership through Athena Cloud Engineers, LLC